COMPARATIVE ANALYSIS OF NANOSCALE COMPARATOR AT 90NM, 65NM AND 45NM FOR DSP APPLICATIONS

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ABSTRACT
In Analog to digital convertor design, high speed comparator influences the overall performance of Analog to Digital Converter (ADC) directly. This paper presents the Comparative analysis of 1um Comparator and 45nm Comparator for ADC .A schematic design of this comparator is given and simulated in HSPICE. Simulation results are compared and presented. The DC Gain, power dissipation, bandwidth, output resistance, Phase margins, slew rate are compared at 1um and 45nm.

Keywords:
Comparator, ADC, Low Power, CMOS Simulation

INTRODUCTION

The comparator is a circuit that compares an analog signal with another analog signal or a reference voltage or signal, and output is a binary signal based on the comparison. The comparator is widely used in the process of converting analog signals to digital signals. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit analog-digital converter. The basic component in ADC device is a comparator. Many comparators have been proposed earlier. Among of these circuits, some are concerned with speed, some emphasizing on low power and high resolution, and some on offset cancellation. Bang-sup Song proposed a comparator circuit with only pre-amplifier and decision stage, but did not provide any experimental results to analyze the circuit performance. Amalan Nag proposed a comparator with 200 MHz speed and with offset cancellation. Allstot also thought of and simulated a novel comparator circuit which has cascading stages and ended up with a minimum power supply requirement of 3.5 V. The resolution may be higher but achieved at the expense of bulky cascading stages.

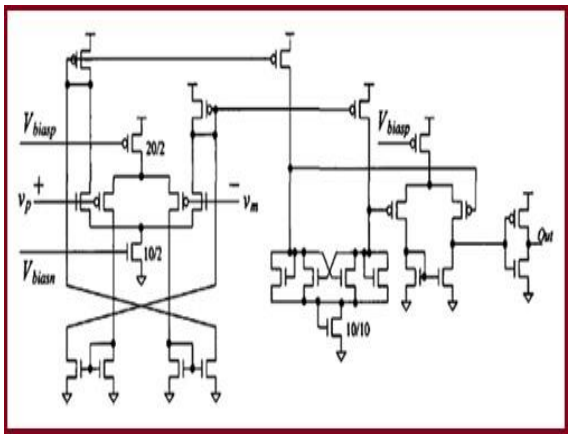
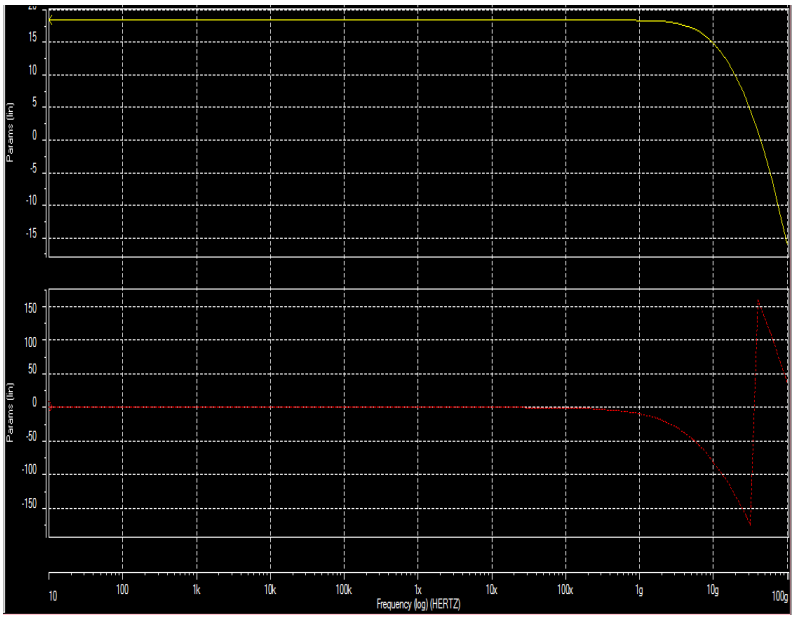


Figure : - Proposed Comparator

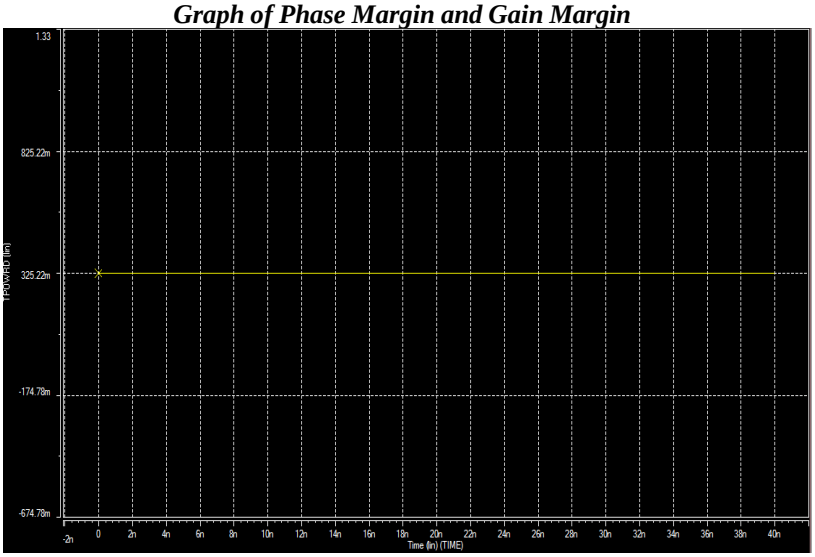
Analysis of The Proposed Comparator

A schematic design of this comparator is given and simulated in HSPICE. Simulation results are compared and presented. The DC Gain, power dissipation, bandwidth, output resistance, Phase margin, slew rate are compared at 1um and 45nm.The performance limiting blocks in ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. To reduce the power consumption and the area of comparators, dynamic comparators are proposed.

Simulation Results of the Proposed Comparator.



Graph of Phase Margin and Gain Margin



Average Power

CONCLUSION

Conclusion and Future Scope of the Work :-

This paper presents a method for design of CMOS comparator based on a pre-amplifier. This paper presents the Comparative Analysis of 1um Comparator and 45nm Comparator for ADC using HSPICE software.

Table: Comparative analysis

S. No.	Parameters	Comparator at 1um	Comparator at 90nm	Comparator at 65nm	Comparator at 45nm
1	DC GAIN	67 dB	13.5 dB	18.84 dB	18 dB
2	DC $GAIN_{max}$	81 dB	18.61 dB	24 dB	23.5 dB
3	3- dB Bandwidth	1.2 E+6Hz	9.74 E+6Hz	2.0762E+07 Hz	8.93 E+9 HZ
4	Output Resistance in Ohms	414	12.52k	4.4257k	111
5	Phase Margin	1549^0	88.3^0	100.85^0	1488^0
6	Supply Voltage	5V	0.82V	0.9V	1.2V
7	Slew Rate(V/us)	1.16E+05	1.12E+06	3.10E+05	6.1387E+05
8	Unity Gain Freq	3.7E+8 Hz	8.48E+7 Hz	3.3E+08 Hz	5.8E+10 Hz

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